UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,561	09/27/2006	Kazumasa Tanida	AI-427NP	5593

23995 7590 10/05/2009

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
ARROYO, TERESA M	
ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
10/05/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,561	TANIDA ET AL.	
	Examiner	Art Unit	
	TERESA M. ARROYO	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/18/09* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/31/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/18/09 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 2, 4, 6, 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Regarding claim 1, the two occurrences of the phrase "when the surface of the solid state device facing the semiconductor chip is viewed from vertically above " renders the claim indefinite because it is unclear whether the limitation(s) preceding the phrase are part of the claimed invention. See MPEP § 2173.05(d).

5. The other claims are rejected as being dependent on an indefinite base claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

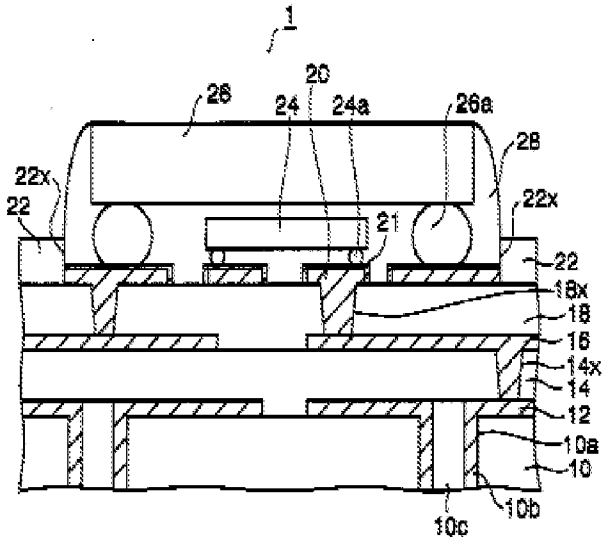
8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1, 2, 4, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Pub. No. 20050067715 to Sunohara in view of US Patent Pub. No. 20040108594 to Toyosawa.

10. Regarding claim 1, Sunohara discloses a semiconductor device, comprising: a solid state device 10; a semiconductor chip 26 having a functional surface on which a functional element 26a is formed, the semiconductor chip 26 being bonded on a surface

of the solid state device 10 with the functional surface thereof facing the surface of the solid state device 10 while maintaining a predetermined distance between the functional surface thereof and the surface of the solid state device 10; an insulating film 22 provided on the surface of the solid state device 10 facing the semiconductor chip 26, the insulating film 26 having an opening greater in size than the semiconductor chip 26 when the surface of the solid state device 10 facing the semiconductor chip 26 is viewed from vertically above; and a sealing layer 28 that seals a space between the solid state device 10 and the semiconductor chip 26.

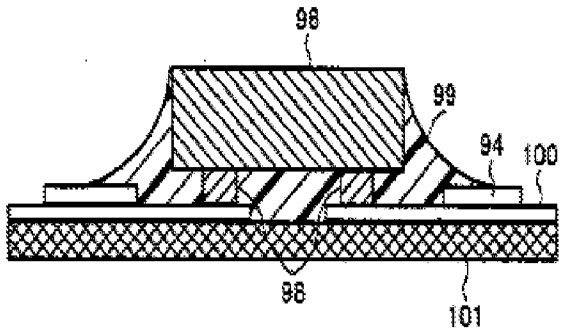
FIG. 3H



11. However, Sunohara does not disclose a pillar-shaped connecting member configured to connect the functional surface of the semiconductor chip to the surface of the solid state device 10, a width of the pillar-shaped connecting member being constant.

12. Toyosawa teaches a pillar-shaped connecting member 98 for connecting a semiconductor chip 96 and a solid state device 10. The width is constant at 24 μm in para. [0135]. Further, Toyosawa teaches a sealing layer 99.

FIG. 2 (b)



13. therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a pillar-shaped connecting member having a constant width in Sunohara such as taught by Toyosawa in para. [0046] since determining the optimum shape/width would have only involved routine skill in the art as discussed in the legal precedent below.

In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966) (The court held that the configuration of the claimed disposable plastic nursing container was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the claimed container was significant.).

14. Regarding claim 2, in both references wherein the sealing layer is provided in such a manner as to fill the opening with the sealing layer.

15. Regarding claim 4, Toyosawa teaches wherein the pillar-shaped connecting member is formed by bonding a connection pad 100 provided on the solid state device 101 and a projection electrode 98 provided on the semiconductor chip 96.

16. Regarding claim 7, both references teach wherein the semiconductor chip is connected in a flip chip manner.

17. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sunohara in view of Toyosawa as applied to claim 1 above, and further in view of US Patent No. 6,281,450 to Urasaki et al.

18. Regarding claim 6, the combination of references fails to teach wherein a distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more when the surface of the solid state device facing the semiconductor chip is viewed from vertically above.

19. Urasaki et al. teach wherein a distance between an outer periphery (1) (boundary of the chip mounting area) of the semiconductor chip (3) and an edge (2) (boundary of the insulating coating) of the opening of the insulating film (6) (insulating coating) is 0.1 mm or more (boundary 2 of the insulating coating 6 is preferably within a range of up to 300 um from the boundary 1 of the semiconductor chip mounting area) when the surface of the solid state device (8) facing the semiconductor chip (3) is viewed from vertically above.

FIG. 3A

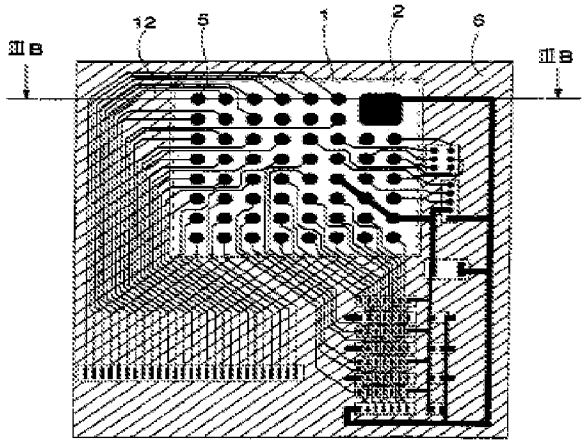
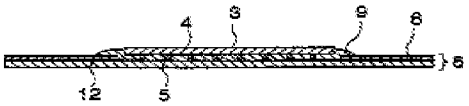


FIG. 3B



20. therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use such a distance in Sunohara since if this boundary-to-boundary distance exceeds 300 μm, the wiring conductors 12 may not be completely covered with the adhesive 9, causing a reduction of insulation reliability as taught by Urasaki et al. in col. 4, lines 31-34.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The other cited prior art on PTO-892 teach a flip chip device including underfill and solder resist.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TERESA M. ARROYO whose telephone number is (571) 272-7260. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. M. A./
Examiner, Art Unit 2826
22.